

170[169]. (Once Amended) The memory of claim 70 wherein said plurality of voltage supplies includes a bias generator for supplying a bias voltage to said array, said bias generator including an output status monitor.

171[170]. (Once Amended) The memory of claim 70 additionally comprising a powerup sequence circuit for controlling the powering up of certain of said plurality of voltage supplies.

172[171]. (Once Amended) The memory of claim 70 wherein said memory provides at least 256 meg of storage.

173[172]. (Once Amended) The memory of claim 172[171] wherein said array provides more than 256 meg of storage, said memory additionally comprising repair logic to logically replace defective memory cells with operable memory cells such that said memory provides said 256 meg of storage.

174[173]. (Once Amended) The method of claim 71 wherein the first external signal is a row address strobe signal and the second external signal is a column address strobe signal.

175[174]. (Once Amended) The method of claim 174[173] wherein writing into subsequent groups of memory elements includes writing into multiple rows in response to each cycle of the column address strobe signal.

176[175]. (Once Amended) The system of claim 100 wherein said array is organized into rows and columns to form a plurality of individual arrays, and wherein said plurality of individual arrays is organized into a plurality of array blocks, and wherein said plurality of peripheral devices includes a plurality of sense amplifiers positioned between adjacent rows of individual arrays and a plurality of row decoders positioned between adjacent columns of individual arrays.

177[176]. (Once Amended) The system of claim 176[175] wherein each of said plurality of individual arrays includes digitlines extending therethrough and into said sense amplifiers, and wherein said array blocks include I/O lines running between adjacent rows of individual arrays and through said sense amplifiers, said sense amplifiers including circuits for transferring signals on said digitlines to said I/O lines.

178[177]. (Once Amended) The system of claim 100 wherein said array of memory cells is organized into a plurality of array blocks, said memory additionally comprising a power distribution bus including a first plurality of conductors forming a web around each of said array blocks and a second plurality of conductors extending from said web to form a grid within each of said array blocks.

179[178]. (Once Amended) The system of claim 178[177] additionally comprising a plurality of pads located centrally with respect to said array blocks, and wherein said power distribution bus includes a third plurality of conductors running parallel to said plurality of pads for receiving an external voltage from said plurality of pads and for distributing the external voltage to said plurality of voltage supplies.

180[179]. (Once Amended) The system of claim 179[178] wherein said array of memory cells is organized into a plurality of array blocks, and wherein said plurality of voltage supplies includes a voltage regulator comprised of a plurality of power amplifiers, and wherein at least one power amplifier is associated with each of said plurality of array blocks.

181[180]. (Once Amended) The system of claim 180[179] additionally comprising circuits for disabling said at least one power amplifier when its associated array block is disabled.

182[181]. (Once Amended) The system of claim 180[179] wherein said plurality of power amplifiers is divided into a plurality of groups for one of separate or concurrent operation to achieve a predetermined level of output power.

183[182]. (Once Amended) The system of claim 100 wherein said plurality of voltage supplies includes a bias generator for supplying a bias voltage to said array, said bias generator including an output status monitor.

184[183]. (Once Amended) The system of claim 100 additionally comprising a powerup sequence circuit for controlling the powering up of certain of said plurality of voltage supplies.

185[184]. (Once Amended) The system of claim 100 wherein said memory provides at least 256 meg of storage.

186[185]. (Once Amended) The system of claim 185[184] wherein said array provides more than 256 meg of storage. said memory additionally comprising repair logic to logically replace defective memory cells with operable memory cells such that said memory provides said 256 meg of storage.

187[186]. (Once Amended) The combination of claim 120 wherein said first external signal includes a row address strobe signal.

188[187]. (Once Amended) The combination of claim 120 wherein said second external signal includes a column address strobe signal.

189[188]. (Once Amended) The method of claim 126 wherein the first external signal is a row address signal and the second external signal is a column address strobe signal.

190[189]. (Once Amended) The method of claim 189[188] additionally comprising the step of writing into subsequent groups of memory elements in response to each cycle of the column addresses strobe signal.

191[190]. (Once Amended) The method of claim 126 wherein said step of latching the data includes the step of connecting each memory element in the first seed group to one of a plurality of sense amps.

192[191]. (Once Amended) The method of claim 191[190] wherein said step of connecting each memory element includes the step of biasing a plurality of isolation transistors into conductive states to connect each memory element in said first seed group to one of the sense amps.

193[192]. (Once Amended) The method of claim 192[191] wherein said step of writing the latched data into a second group of memory elements includes the step of connecting each memory element in the second group to one of the sense amps.

194[193]. (Once Amended) The method of claim 193[192] wherein said step of connecting each memory element in the second group includes the step of biasing a plurality of isolation transistors into conductive states to connect each memory element in the second group to one of the sense amps.

195[194]. (Once Amended) The method of claim 142 wherein the receipt of the sequence of a write enable signal, column address strobe signal and a row address strobe signal enables the detector.

196[195]. (Once Amended) The method of claim 143 wherein said step of enabling a detector is performed by the step of inputting a sequence of control signals.

197[196]. (Once Amended) The method of claim 196[195] wherein said sequence of control signals includes a write enable signal, column address strobe signal and row address strobe signal.

198[197]. (Once Amended) The method of claim 143 wherein said step of inputting at least one address to the device is performed while said step of inputting a voltage is performed.

199[198]. (Once Amended) The method of claim 143 wherein said step of inputting at least one address includes the step of inputting a first address for confirming that the device is to be in a test mode and inputting a second address for specifying a test mode.

200[199]. (Once Amended) The method of claim 147 additionally comprising the step of inhibiting the device from normal operation while said step of applying a voltage is performed.

201[200]. (Once Amended) The method of claim 147 additionally comprising the step of ending the application of a voltage outside the range of voltages used to represent logic signals to take the device out of a test mode.

202[201]. (Once Amended) The method of claim 147 additionally comprising the step of inputting an address containing information to take the device out of a test mode.

203[202]. (Once Amended) The method of claim 152 wherein the step of applying a voltage includes the step of applying a voltage higher than the highest voltage used to represent logic signals in the device.

204[203]. (Once Amended) The method of claim 152 additionally comprising the step of inhibiting the device from normal operation while said step of applying a voltage is performed.

205[204]. (Once Amended) The method of claim 152 additionally comprising the step of ending the application of a voltage outside the range of voltages used to represent logic signals to take the device out of a test mode.

206[205]. (Once Amended) The method of claim 152 additionally comprising the step of inputting a clear test mode key to take the device out of a test mode.